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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,058	10/29/2001	David J. Musliner	H0001845 (FSP:114.002US01)	7009
7590	02/22/2005			EXAMINER
Honeywell International Inc. Law Dept. AB2 P.O. Box 2245 Morristown, NJ 07962-9806			PALADINI, ALBERT WILLIAM	
			ART UNIT	PAPER NUMBER
			2125	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/015,058	MUSLINER ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 29 October 2001.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/29/01.

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_ .

**DETAILED ACTION*****Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With respect to figure 4, lines 19-20 on page 7 state, "That a state has already been visited indicates that all of the states are good." According to this statement, once the first state has been visited, it may be assumed that all other states are good. It would appear that the other states must be visited to determine if they are good.

Appropriate correction and clarification is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hardin (6102959).

In figure 2, Hardin discloses a method for formal verification of a system design where the first verification of the system is verified in block 23 after the first iteration. Under-defined states are determined and reported in block 24. The loop continues through successive states from decision block 25 back to the input of block 22, where newly specified states are generated to continue in the loop to successor states. A second verification is performed in block 23, and the loop continues through successive verifications.

5. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Alur (5483470).

In figure 2 Alur discloses a method and system for verification, where the user provides a high level definition of the system to be designed to block 13 and this is fed to the verification block 14. At the next iteration, the user inputs a refined definition of the system into block 13 and a mapping, which maps the states and actions at the states, of the system specification in block 15 to the states and actions at the states of the system specification in block 13. The state-to-state mapping is depicted in figure 3.

Figure 6 shows the determination of a bad or undefined state in block 54.

***Relevant Prior Art***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Loyer (5291427) discloses a method for developing communication automata which includes a number of operations where after each combination operation a resulting net is subject to an analysis to verify that the properties obtained match the properties required by the designer and to determine a reachability graph. The development machine using conventional Petri net computation methods effects the determination and verification simultaneously. This analysis is dynamic and exhaustive, i.e. it looks for all possible transitions and states in the net resulting from the combination. It deduces from this graph the general properties of the net and in particular verifies if it is: bounded, safe, live, proper and deadlock-free. In the preferred embodiment, a second stage of Petri net combination is, for each interface external to the set of automata and for each inter-automaton interface, to effect the combinations using the asynchronous communication mode to combine Petri nets replacing initial nets with each other or with an existing initial net, if any, to obtain from each combination a Petri net modeling communication between two automata or between an interface external to an automaton and the environment of that automaton.

Peled (6526544) discloses a system and method for verification of a black box, without utilizing all of the states and state transitions, where one embodiment entails a series of experiments on the black box to verify if the box exhibits the desired property. In another embodiment, the experiments are used to build a model of the black box by monotonically incrementing that states of a conjectured automaton until the conjectured automation and the black box converge or an error is discovered. Convergence is verification.

Morely discloses a system for analyzing temporal expressions resulting in the construction of a finite state machine. A deterministic or non-deterministic state machine is constructed for applications such as the examination of the temporal behavior of a device under test. Temporal expression evaluation starts during program execution, and continues over a number of clock cycles, and success is defined as the preceding sequence of program states satisfy the mathematical definition of the temporal expression.

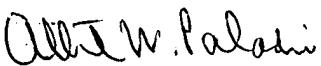
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7. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (571) 272-3748. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (571) 272-3749. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

February 18, 2005

  
Albert W. Paladini  
Primary Examiner  
Art Unit 2125